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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,662	06/19/2001	Hiroshi Takahashi	TIJ-29232	4499

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,662	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 6-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *15 July 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Acknowledgement

Receipt is acknowledged of the Amendment filed September 8, 2003.

Claim Objections

Claims 4, 8, 12, 15, 16, and 17 are objected to because of the following:

Claim 4 depends on canceled claim 3. It appears that it should depend from claim 1. On line 1-2, "other of said MOS transistors" should be changed to --MOS transistor--; on line 2, "a PMOS" should be changed to --an NMOS--; on line 3, "an NMOS" should be changed to --a PMOS-- in order to avoid confusion and have a clear antecedent basis because there are two "other" transistors.

Claim 8, line 6, "the other of said complementary serially connected MOS transistors" lack antecedent basis. It should be changed to --the first MOS transistor--.

Claim 12 is an exact duplicate of claim 10. Claim 12 should depend from claim 11.

Claim 15, line 1, --first-- should be inserted after "wherein the"; and line 3, --of the bias voltage supply circuit-- should be inserted between "transistor" and "are"

Claim 16, line 2, --of the logic circuit-- should be inserted between "PMOS transistor" and "and a" in order to have a clear antecedent basis.

Claim 17, lines 4-5, "the other of said complementary serially connected MOS transistors" lack antecedent basis. It should be changed to --the first MOS transistor--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-2, 4, and 6-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Koga (US 6,191,615 B1).

Regarding claims 1, 8, and 11, in Fig. 1, Koga which was cited previously but not relied upon, teaches, a semiconductor device comprising:

a logic circuit (100) comprising a first MOS transistor (MP11) and a second MOS transistor (MN11) connected in series between the supply line of a power supply voltage (VDD11) and ground potential (GND11), a substrate region of said second MOS transistor being permanently coupled (not directly coupled but permanently coupled via 10) to ground potential, the second transistor having a lower leakage and driving current and higher threshold voltage than the first MOS transistor (when MN11 is ON and MP13 is ON);

a first bias voltage supply circuit (20), which selectively supplies a first bias voltage (VDD11 via MP12) or a second bias voltage (VDD12 via MP13) which are different from each other (col. 4, lines 24+) to the substrate region of the first MOS transistor.

Regarding claim 17, Koga teaches, in Fig. 1, a semiconductor device comprising:

a logic circuit (100) comprising a first MOS transistor (MP11) and a second MOS transistor (MN11) connected in series between the supply line of a power supply voltage

(VDD11) and ground potential (GND11), the second transistor having a lower leakage and driving current and higher threshold voltage than the first MOS transistor (when MN11 is ON and MP13 is ON);

a first bias voltage supply circuit (20), which selectively supplies a first bias voltage (VDD11 via MP12) or a second bias voltage (VDD12 via MP13) which are different from each other (col. 4, lines 24+) to the substrate region of the first MOS transistor; and

a second bias voltage supply circuit (10), which selectively supplies a first bias voltage (GND12 via MN13) or a second bias voltage (GND11 via MN12) which are different from each other (col. 4, lines 9+) to the substrate region of the second MOS transistor.

Regarding claims 2, 13, 22, 23, and 24, Koga teaches, in Fig. 1, that the first bias voltage supply circuit includes a first MOS transistor (MP12) connected between a first voltage supply line (VDD11) and a bias voltage supply line (N11) and a second MOS transistor (MP13) connected between a second voltage supply line (VDD12) and the bias voltage supply line (N11), and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor; and wherein the second bias voltage supply circuit (10) includes a third MOS transistor (MN12) connected between the substrate of the second MOS transistor (MN11) of the logic circuit and ground potential (GND11) and a fourth MOS transistor (MN13) connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line (GND12).

Regarding claims 4, 9, and 18, Koga teaches, in Fig. 1, that the first MOS transistor is a PMOS transistor (MP11) and the second MOS transistor is an NMOS transistor (MN11).

Regarding claims 6 and 28, Koga teaches, in Fig. 1, that one said bias voltage (VDD11 via MP12 > Vth of MP11) is above the threshold voltage (Vth of MP11) of said first MOS transistor and the other said bias voltage (VDD12 via MP13 = 0 V since MP13 is off) is below the threshold voltage of said first MOS transistor.

Regarding claims 7, Koga teaches, in Fig. 1, that at least one additional logic circuit (10) coupled to the bias voltage supply circuit.

Regarding claims 10, 12, and 19, Koga teaches, in Fig. 1, that the first bias voltge (VDD11) from the first bias supply circuit is lower than (col. 4, lines 24+) the second bias voltage (VDD12) from the first bias supply circuit.

Regarding claims 14, Koga teaches, in Fig. 1, that the MOS transistor of the logic circuit is connected to the first voltage supply line (VDD11).

Regarding claims 15, 25, 26, and 27, Koga teaches, in Fig. 1, that the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors (MP12, MP13) and the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors (MN12, MN13).

Regarding claims 16, Koga teaches, in Fig. 1, that the logic circuit includes an NMOS transistor (MN13) connected between the PMOS transistor of the logic circuit and a third voltage supply line (GND12).

Regarding claims 20, Koga teaches, in Fig. 1, that the first bias (GND12 via MN13) voltage from the second bias supply circuit is lower than (col. 4, lines 9+) the second bias voltage (GND11 via MN12) from the second bias supply circuit.

Regarding claims 21, Koga teaches, in Fig. 1, that the first MOS transistor (MP11) has a lower threshold voltage (when MP11 is ON and MN13 is ON) than said second MOS transistor (MN11).

Response to Arguments

Applicant's arguments with respect to claims 1-2, 4, and 6-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

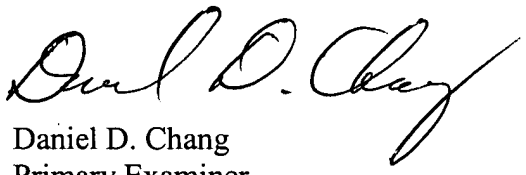
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Daniel D. Chang
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Art Unit 2819

DC

DANIEL CHANG
PRIMARY EXAMINER